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In this research we have investigated parallel algorithms for placement, routing, layout verification and extraction, logic synthesis, test generation, and fault simulation, and behavioral simulation. The parallel algorithms have been designed such that they are portable across a range of parallel machines, including multiprocessor workstations, shared memory multiprocessors, message passing multiprocessors, and networks of workstations. The algorithms have been designed to run on top of the ProperCAD2 C++ library as well as the Message Passing Interface (MPI).

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VLSI CAD ON SCALABLE HIGH-PERFORMANCE COMPUTING PLATFORMS

FINAL PROGRESS REPORT

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A. STATEMENT OF THE PROBLEM STUDIED

The objectives of this research are to develop efficient parallel algorithms for VLSI CAD tasks that can utilize the computing power of a wide range of parallel platforms that are becoming available to the community, with the eventual goal of reducing the design turnaround time of complex chips of the future.

In this research we have investigated parallel algorithms for placement, routing, layout verification and extraction, logic synthesis, test generation, and fault simulation, and behavioral simulation. The parallel algorithms have been designed such that they are portable across a range of parallel machines, including multiprocessor workstations, shared memory multiprocessors, message passing multiprocessors, and networks of workstations. The algorithms have been designed to run on top of the ProperCAD2 C++ library as well as the Message Passing Interface (MPI).

B. SUMMARY OF MOST IMPORTANT RESULTS

Accomplishment 1

Our parallel algorithms for placement are based on simulated annealing. Several parallel algorithms have been pursued. The ProperPLACE-PM algorithm is based on having different processors perform moves in parallel on different cells in the design. The cells are partitioned among the processors, but can be moved anywhere in the chip image. A second strategy ProperPLACE-SC is to use speculative execution on the moves. The idea is to view the simulated annealing algorithm as a set of moves that are accepted and rejected. Each processor pursues speculatively to assume that some sequence of moves will be accepted or rejected. A third strategy called ProperPLACE-MMC is based on multiple Markov chains. The idea is to have different processors perform completely independent simulated annealing with different random seeds and periodically exchange the solutions. We have obtained portable parallel implementations on each of the above approaches. Speedups of 6.5 on 8 processors have been obtained using the ProperPLACE-MMC algorithm with less than 3% degradation in quality of solutions. Speedups of 4.5 on 8 processors have been obtained with the ProperPLACE-PM schemes with about 5-10% degradation in quality of solutions. No speedups have been obtained with the ProperPLACE-SC scheme since the cost of communication dominated the computation. In addition to the above algorithms, a new circuit partitioned algorithm for standard cell placement, called ProperPLACE-PART, has been developed which can run on very large problems that do not run on a single processor due to memory limitations. Each processor performs annealing based moves on cells in its current set of cells but moves them all across the circuit. Periodically, the cell partitioning across the processors is changed. This circuit-partitioned approach provides speedups to larger number of processors with little loss of qua lity with excellent memory scalability. Speedups of about 6 on 8 processors of a SPARCSERVER-1000 and about 11 on 32 processors of a CM-5 have been measured for the algorithm. The quality of the solutions of the parallel algorithm are within 5% of the sequential algorithms. The strength of this memory scalable algorithm is that one can run placement on circuits that do not fit on the memory of a single processor.

Accomplishment 2

We have developed various parallel algorithms for global routing of standard cell designs based on the Timberwolf 6.0 global router. We have developed three different approaches for parallelizing the global routing problem. The first approach partitions the nets across the processors, and each processor performs a global routing in parallel. The second approach partitions the chip area among the processors by rows, and each processor performs routing of all the nets belong to its region. A third approach uses a hybrid approach where part of the algorithm is performed using net decomposition, and part of the algorithm is performed using an area decomposition. We have experimentally evaluated the performance of all three parallel algorithms. The hybrid algorithm has been found to obtain the best speedups (about 6.5 on 8 processors on a SUN SparcCenter 1000) and has minimized the quality degradation of the routing to less than 2% of the serial algorithm for various benchmark circuits.

Accomplishment 3

We have developed three parallel layout verification algorithms for mask layouts. The first algorithm called ProperDRC1 uses data parallelism to distribute rectangles of a mask layout to different processors. The second algorithm called ProperDRC2 uses task parallelism to assign different design rules to different

processors. A third algorithm combines task and data parallelism to combine the benifits of both approaches. Speedups of about 100 have been obtained on 128 processors of a CM-5.

Accomplishment 4

Our parallel algorithm for logic synthesis is based on the MIS/SIS approaches developed by researchers at Berkeley. We have developed parallel algorithms for several key transformations in combinational logic synthesis, specifically, kernel extraction, cube extraction, node resubstitution, and node simplification. We have obtained excellent parallel implementations of the parallel MIS algorithm. Speedups of 6.0 have been obtained on 8 processors in the parallel implementations on a Sun SparcCenter 1000.

In addition to the above algorithms, three different algorithms for the algebraic factorization procedures in combinational logic synthesis within the MIS system have been developed. The first algorithm uses circuit replication and uses a divide-and-conquer strategy to follow the same search path as the sequential algorithm. A second algorithm uses totally independent factorization on different circuit partitions, A third algorithm uses a novel L-shaped partitioning strategy which allows for some interaction among the kernels in various partitions. All the algorithms have been implemented on a SUN SPARCSERVER 1000. For a large circuit having 14,000 literals, the third algorithm runs 11.5 times faster than the sequential algorithm with less than 0.2% degradation in the quality of the results.

Accomplishment 5

In the area of sequential logic synthesis, two novel parallel algorithms for state-assignment of finite state machines have been developed: one based on MUSTANG called ProperSTATE, another based on JEDI called ProperJEDI, which are part of the SIS synthesis tool. Both algorithms have been developed in a data-partitioned manner so that they are both processor and memory scalable for very large finite state machines, namely they can perform state assigment on examples that do not run on a single processor, but run across the memory of a parallel machine. Speedups of about 7 on an 8-processor SPARCSERVER-1000 and about 30 on a 64-processor CM-5 have been measured for both algorithms. The quality of the solutions of the parallel algorithm are within 1% of the sequential algorithms. In the area of FPGA synthesis, we have developed a parallel algorithm for technology mapping of look-up table based FPGAs. Speedups of 6.5 on 8 processors have been obtained on various benchmark circuits on a SUN SPARCCENTER 1000 multiprocessor. This algorithm will enable the state assignment of finite state machines having 200 latches and beyond which will push the current state of the art from about 20 latch circuits.

Accomplishment 6

Three new parallel test generation algorithms for sequential circuit test generation based on a genetic algorithm called GATEST have been developed. The first algorithm called ProperGATEST1 performs parallelization using data decomposition by partitioning the populations in the genetic algorithm across the processors, and obtains speedups of about 6.8 on 8 processors of a SPARCSERVER-1000. These results have been reported without any degradation in the quality of the solutions from the sequential algorithm. The second algorithm, ProperGATEST2, uses a parallel search strategy where each processor executes the sequential genetic algorithm with a different seed, and uses migration to share information between processors. Speedups of about 5.3 on 8 processors have been obtained on a SUN SPARCSERVER 1000 with qualities that are comparable to the serial algorithm. The third algorithm, ProperGATEST3, is a subpopulation based version of ProperGATEST2, where subpopulations are distributed across processors and information is migrated from one processor to another. Speedups of about 7.2 on 8 processors have been obtained on a SUN SPARCSERVER 1000 with qualities that are comparable to the serial algorithm. These algorithms will enable the generation of tests for very complex circuits of the future.

Accomplishment 7

We have developed various parallel algorithms for fault simulation. While previous approaches to parallel fault simulation have used circuit parallelism or fault parallelism approaches, in the past year, we have developed scalable parallel test-set partitioned algorithms for fault simulation in a series of implementations called SPITFIRE. The basic idea in this approach is to partition the test sets among the processors so that each processor performs fault simulation on its own set of inputs but on the entire circuit and on the entire list of faults. While this approach is easily applicable to combinational circuits, the approach is not directly applicable in sequential circuits where there are state dependencies across time frames, i.e. the state of the circuit at the present time frame may depend on the state of the circuit in all previous time frames. We proposed a technique of allowing for some overlaps of test vectors among the different test partitions in the

various processors. By experimenting with the degree of overlap, it was possible to control the quality of the results (fault coverage) and the speedups obtained. We developed six variants of this algorithm and one of those actually combined fault parallelism and test set parallelism very effectively. The most efficient algorithms produced average speedups of about 6.5 on 8 processors of a SPARCServer 1000 multiprocessor on several large sequential benchmarks.

Accomplishment 8

We have developed an efficient compiled event-driven simulation algorithm for VHDL simulations. Two approaches to parallelization on shared memory multiprocessors were developed. The first one was based on fine grained task scheduling where each task corresponded to a straightline sequence of VHDL code without any wait statements. The second appproach was based on a coarse grained partitioning of the program by identifying fan-in cones of the circuits being simulated. Both approaches were evaluated on a set of benchmark examples. Speedups of about 3 to 4 were meaasured on 8 processors of a SUN SPARCServer 1000 multiprocessor.

Accomplishment 9

We have developed several parallel algorithms for high-level synthesis of signal flow graphs. One set of parallel algorithms have been developed for the force directed scheduling problem by partitioning the nodes and time steps across the processors. Speedups of about 4 have been measured on 8 processors of an SGI Origin, and about 8 on 16 processors of an IBM SP2. Another set of parallel algorithms have been based on a multiple Markov Chain model of parallel simulated annealing which simultaneously tries to perform scheduling, allocation and floorplanning. Speedups of about 14 have been reported on several benchmark circuits on 16 processor of an IBM SP2 multiprocessor.

Accomplishment 10

We have developed several parallel algorithms for power estimation of combinational and sequential circuits based on exhaustive simulation and Monte Carlo methods. Speedups of about 14 on 16 processors were obtained for combinational circuits and about 10 on 16 processors for sequential circuits on an IBM SP2 multiprocessor.

Accomplishment 11

Finally, we have developed parallel algorithms for 3-dimensional circuit extraction of interconnect structures based on the Boundary Element Method. We have developed parallel algorithms for constructing the matrix of the BEM method and for solving the equations based on both direct and indirect methods. Speedups of about 12 on 16 processors of an IBM SP2 multiprocessor have been reported.

TECHNOLOGY TRANSFER

The ProperCAD library that was originally developed at the University of Illinois has been licensed to a commercial company, Sierra Vista Research (SVR). In cooperation with the University of Illinois, SVR has provided improvements to the interfaces to the ProperCAD library, and some documentation on how to use the library. The library is now commercially available from Sierra Vista Research.

The parallel design rule checking algorithms developed as part of the project has been transferred to Cadence Design Systems . They have employed the concepts of parallel layout verification within their DRC tool called VAMPIRE. It is now a commercial product.

The parallel placement algorithms developed as part of this project have been transferred to LSI Logic Corporation. They have used the concepts of parallel simulated annealing in placement within their placement tool called CMDE-PLACE.

The parallel logic synthesis algorithms developed as part of this contract have been transferred to Ambit Design Systems and have been incorporated into their commercial package called BuildGates.

C. LIST OF ALL PUBLICATIONS AND TECHNICAL REPORTS

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D. LIST OF ALL PARTICIPATING SCIENTIFIC PERSONNEL

D.1. University of Illinois

- PROF. PRITHVIRAJ BANERJEE, Professor, Electrical and Computer Engineering, Coordinated Science Lab, University of Illinois, Urbana.
- PROF. JANAK PATEL, Professor, Electrical and Computer Engineering, Coordinated Science Lab, University of Illinois, Urbana.
- DR. BALKRISHNA RAMKUMAR, Postdoctoral Researcher, Coordinated Science Lab, University of Illinois, Urbana.
- PRADEEP PRABHAKARAN, Ph.D. Student, Electrical and Computer Engineering, University of Illinois (Advisor: P. Banerjee), graduated 9/98, presently working for *Compaq-Digital*
- SUMIT ROY, Ph.D. Student, Electrical and Computer Engineering, University of Illinois (Advisor: P. Banerjee), graduated 8/98, presently working for *Ambit Design Systems.*
- DANIEL PALERMO, Ph.D. Student, Electrical and Computer Engineering, University of Illinois (Advisor: P. Banerjee), graduated 5/96, presently working for *Hewlett-Packard Convex.*
- GAGAN HASTEER, Ph.D. Student, Computer Science, University of Illinois (Advisor: P. Banerjee), graduated 12/97, presently working for *Ambit Design Systems.*
- ERNESTO SU, Ph.D. student, Electrical and Computer Engineering, University of Illinois (Advisor: P. Banerjee), graduated 3/97, presently working for *Intel Corporation.*
- JOHN HOLM, Ph.D. Student, Electrical and Computer Engineering, University of Illinois (Advisor: P. Banerjee), graduated 4/97, presently working for *Intel Corporation.*
- VENKAT KRISHNASWAMY, Ph.D. Student, Computer Science, University of Illinois (Advisor: P. Banerjee), graduated 4/97, presently working for *Intel Corporation.*
- DILIP KRISHNASWAMY, Ph.D. Student, Electrical and Computer Engineering, University of Illinois (Advisor: P. Banerjee), graduated 7/97, presently working for *Intel Corporation.*
- ZHAOYUN JASON XING, Ph.D. Student, Computer Science, University of Illinois (Advisor: P. Banerjee), graduated 7/97, presently working for *SUN Microsystems.*

D.2. Northwestern University

The subcontract to Northwestern University supported the following Ph.D./M.S. Students in the ECE department at Northwestern.

- DHRUVA RANJAN CHAKRABARTI Ph.D. Student, Electrical and Computer Engineering, Northwestern University, (Advisor: P. Banerjee), Expected graduation 8/99.
- YANHONG YUAN, Ph.D. Student, Electrical and Computer Engineering, Northwestern University, (Advisor P. Banerjee), Expected graduation 8/99.
- JER-SHENG CHEN, Ph.D. Student, Electrical and Computer Engineering, Northwestern University, (Advisor P. Banerjee), Expected graduation 8/00.
- JIWOONG VICTOR KIM, M.S./Ph.D. Student, Graduated M.S. May 1998, Electrical and Computer Engineering, Northwestern University, (Advisor P. Banerjee), Expected graduation 8/00.
- PRAMOD JOISHA, M.S./Ph.D. Student, Electrical and Computer Engineering, Northwestern University, (Advisor P. Banerjee), Expected graduation 8/01.

D.3. Subcontract to Sierra Vista Research

- Dr. STEVEN PARKES, Sierra Vista Research, San Jose, CA.

D.4. Subcontract to Cadence Design Systems

- DR. EDWIN PETRUS, Cadence Design Systems

D.5. Subcontract to LSI Logic

- Dr. SUNGHO KIM, LSI Logic

E. HONORS RECEIVED

- Prof. Banerjee was awarded the *Best Paper Award* at the IEEE VLSI Test Symposium, Monterey, CA, April 1998.
- Prof. Banerjee received the *1996 Frederick Emmons Terman Award* from the ASEE's Electrical Engineering Division, sponsored by Hewlett-Packard Company, presented to an Outstanding Young Electrical Engineering Educator, for publishing the textbook "Parallel Algorithms for VLSI CAD".
- Prof. Banerjee became Fellow of IEEE, 1995
- Prof. Banerjee was invited to give the Keynote Address at the International Conference on Parallel and Distributed Systems, New Orleans, in October 1997.
- Prof. Banerjee was hired as Walter P. Muprhy Chaired Professor of Electrical and Computer Engineering, Northwestern University,m Sep. 1, 1996.